WHAT IS CLAIMED IS:

1. A random access memory device comprising:

a memory array having a plurality of memory cells configured to hold a charge;

a command block coupled to the memory bank and configured to receive refresh commands used to periodically refresh the memory cells; and

a detection circuit coupled to the command block and to the memory array, the detection circuit configured to store a hit detect signal when the memory array is accessed, and receive the refresh command including enabling block select signals only when the hit detect signal is stored while the refresh command is received.

2. The random access memory device of claim 1 wherein the memory array is contained in a memory bank, the random access memory device having multiple memory banks and multiple memory arrays within each memory bank.

3. The random access memory device of claim 1 wherein the detection circuit is configured with a latch to store the hit detect signal when a memory array is accessed.

4. The random access memory device of claim 3 further including an enable circuit coupled to the latch and configured to receive the refresh command such that the enable circuit enables block select signals when the hit detect signal is stored while a refresh command is received and disables block select signals when the hit detect signal is not stored while a refresh command is received.

5. The random access memory device of claim 1 further comprising an address block configured to receive address information.

6. The random access memory device of claim 5 further comprising a row decoder block coupled to the address block to receive row address information, wherein the detection circuit is within the row decoder block.

7. The random access memory device of claim 6 wherein the address information received by the address block comprises a number of bits, some of which identify a memory array within a memory bank, these bits also received by the detection circuit such that the detection circuit can store information indicative of which memory arrays have been accessed.

8. The random access memory device of claim 1 wherein the detection circuit is configured to receive an active command signal indicative of whether a memory array has been activated and a refresh signal indicative of whether a refresh command has been given.

9. The random access memory device of claim 3 wherein the detection circuit further includes a reset circuit configured to reset the stored hit detect signal each time the memory device powers up and each time the memory device enters a deep power down mode.

10. A semiconductor memory device comprising:

at least one memory bank having multiple memory array blocks, the memory array blocks each having multiple memory cells with a unique column and row address, each cell configured to hold a charge;

an address block coupled to the memory bank and configured to receive address information;

a row decoder block coupled to the address block to receive row address information;

a command block coupled to the memory bank and configured to receive refresh commands that are used to periodically refresh the charge in the memory cells; and

a block hit detection circuit within the row decoder block, the block hit detection circuit including a latch to store a hit detect signal when an array block is accessed, and including an enable circuit coupled to the latch and configured to receive the refresh command such that the enable circuit enables block select signals when the hit detect signal is stored while a refresh command is received and does not enable block select signals when the hit detect signal is not stored while a refresh command is received.

11. The semiconductor memory device of claim 10 wherein the memory address comprises a plurality of bits and wherein the block hit detection circuit is responsive to the less than all of the bits of the memory address.

12. The semiconductor memory device of claim 11 wherein the bits of the memory address that the hit detection circuit is responsive to identify one particular array block within one particular memory bank.

13. The semiconductor memory device of claim 10 wherein the block hit detection circuit further includes a gate circuit configured to receive an active command signal indicative of whether an array block has been activated, a refresh signal indicative of whether a refresh command has been given, and an inverse to the hit detect signal indicative of whether the hit detect signal has been stored.

14. The semiconductor memory device of claim 13 wherein the gate circuit allows storage of the hit detect signal when a selected array block has been activated, when no refresh command is present, and when no hit detect signal has already been stored.

15. The semiconductor memory device of claim 13 wherein the gate circuit does not allow storage of the hit detect signal when no selected array block has

been activated, or when a refresh command is present, or when the hit detect signal has already been stored.

16. The semiconductor memory device of claim 10 wherein the block hit detection circuit further includes a reset circuit configured to reset the stored hit detect signal each time the memory powers up and each time the memory enters a deep power down mode.

17. A method of decreasing current consumption in a dynamic memory device, the method including the steps of:

providing a semiconductor memory device with at least one memory bank having multiple memory array blocks, each memory array having a plurality of memory cells;

performing write operations on the memory device such that data is written to the cells within the memory array blocks;

tracking when a memory array block is accessed for storing data and then storing a record of this array block access;

periodically refreshing the memory in order to retain data; and

utilizing the stored record of array block access to prevent refreshing of array blocks that have not been accessed and allowing refreshing of array blocks that have been accessed.

18. The method of claim 17 further including the step of resetting the stored record of array block access after the dynamic memory device is powered up.

19. The method of claim 17 further including the step of resetting the stored record of array block access after the dynamic memory device enters a deep power down mode.

20. A semiconductor memory device comprising:

a memory array having a plurality of memory cells configured to hold a charge;

means coupled to the memory bank for receiving refresh commands used to periodically refresh the memory cells; and

means coupled to the command block and to the memory array for storing a hit detect signal when the memory array is accessed, for receiving the refresh command, and for enabling block select signals only when the hit detect signal is stored while the refresh command is received.